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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
QUILLEN, ALLEN E	

ART UNIT	PAPER NUMBER
2676	11

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,043	DOTSON, GARY DAN	
	Examiner	Art Unit	
	Allen E. Quillen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Pages 9-12, filed February 6, 2004, with respect to Claims 1-30 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art that explicitly discloses the FIFO underflow indication with first input and output counter values.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-11, 17-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al, U.S. Patent 5,953,020, Valmiki et al, U.S. Patent 6,661,422, Duzan, U.S. Patent 5,214,607.

4. Regarding claim 1, representative of claims 17, 25, 30, Wang discloses a first in first out (FIFO) memory (Figure 2, element 70, Column 4, line 50) that interfaces a host bus (Figure 2, element 18, Column 3, lines 57-59) in with the raster engine (*CRT controller,* Figure 2, element 42, Column 4, lines 19-22) and adapted to obtain video data (Column 4, lines 8, 13, 15, *video clock, pixel data*) from the frame buffer (Figure 2, element 16, Column 4, lines 41-42).

Wang discloses a counter that has a value indicative of video data obtained from the frame buffer (Figure 2, elements 16, 18, 32, 56, 58, 78, *read and write pointers*, Column 4, lines 25-34); a counter (Figure 3, element 84) that has a value indicative of video data, provided to the video [memory] (Figure 3, elements 16, [**note element 62**], *pixel data,* 68, 80, ***indicates*** *the entry status,* Column 5, lines 22 through Column 6, line 66); and a control logic system (Figure 2, elements 78,) associated with the FIFO memory, that provides an underflow (and overflow) indication (Figure 2, see Frame buffer above, *fill and drain standpoint,* Column 5, lines 22-26; *underflow (and overflow)*, Column 6, lines 65-66).

[Further claims 25, 30] Wang discloses performing a comparison [based on] input and output counter values and that the underflow indication is controlled according to counter values (see above, *threshold watermark,* Column 8, lines 21-30).

Wang discloses a frame buffer memory but does not explicitly disclose a video controller raster engine in the computer system that receives video data and renders formatted data to a display in a computer system from [an external memory] via the host bus and to provide video data to a video pipeline. Valmiki teaches a video controller raster engine in the computer system (Figures 1-5, 46, Column 80, lines 37-68; Column 88, lines 34-65; Column 90, lines 31-43; Column 95, lines 30-67) that receives video data and renders formatted data (...*decoded MPEG*

signals or other format of digital video, Column 5, lines 21-29) to a display in a computer system (Figure 1, element 22; Figure 2, element 58;) from the frame buffer via the host bus and to provide video data to a video pipeline (see above, Figure 4, element 82, Column 8, lines 5-6). The motivation for combining a video first-in-first out (FIFO) memory with a computer rendering system is to manage the priority of memory requests tasks in a high-definition video application (Column 53 through Column 70) in order not to starve or overfill the display memory (Column 56, lines 2-9). Valmiki is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing MPEG high-definition video machines, to combine the benefits of a video first-in-first out (FIFO) memory, as Wang discloses, with a computer MPEG video rendering system, as Valmiki teaches, to manage priorities of memory requests in order not to starve or overfill the display memory.

Wang discloses a counter is used in the filling and draining of video data in the actual FIFO that has an emulator that "indicates the entry status of the actual FIFO from a fill and drain standpoint." (See above). Wang also discloses that a counter is used in the logic (Figures 5-7) of controlling the watermark threshold in the input from the frame buffer to the FIFO and the output of the FIFO to the display (See Figure 2, elements 32, 36; Figure 4, elements 80, 82, *write request to fill the FIFO, display FIFO memory*, element 70; Column 8, line 31 through Column line 23).

Wang does not disclose a first input counter nor a first output counter. Duzan teaches a first input [READ to the FIFO] counter and a first output [WRITE from the FIFO] counters (Figure 2, elements 80 and 90, Column 3, lines 48-62, *Each clock cycle defines a FIFO memory period. For every byte that is READ from the FIFO, a count of the number of FIFO bytes stored*

is reduced by one byte. Similarly, for every byte that it WRITTEN from the FIFO, the count of the number of FIFO bytes stored is increased by one byte.) The motivation for combining a video first-in-first out (FIFO) memory with a first input counter and a first output counter is, for each clock cycle, to monitor for preventing overflow threshold condition, data overflow and underflow problems in the FIFO, a time-buffer to compensate for different systems components that operate on different data or clock rates (Column 1, lines 9-57; Abstract). Duzan is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing MPEG high-definition video machines, to combine the benefits of a video first-in-first out (FIFO) memory, as Wang discloses, with first input and first output counters, as Duzan teaches, to monitor the FIFO overflow and underflow during each FIFO clock cycle.

5. Regarding claim 2, representative of claim 4, Wang and Valmiki disclose a raster engine of claim 1, wherein Wang discloses the underflow indication comprises an underflow signal (Figure 3, element 62, Column 5, lines 2-8) indicating at least one of an existing underflow condition (*Continually shows how many memory clocks are left over*, Column 6, lines 41-44), an anticipated underflow condition (*drain rate determinator*, Column 6, lines 5-11; *cycles to drain FIFO*, Figure 5, element 118), and a raster engine lockup condition (Column 5, lines 22-26; Column 6, lines 65-66).

Wang does not disclose a first input counter nor a first output counter. Duzan teaches a first input [READ to the FIFO] counter and a first output [WRITE from the FIFO] counters (Figure 2, elements 80 and 90, Column 3, lines 48-62, *Each clock cycle defines a FIFO memory period. For every byte that is READ from the FIFO, a count of the number of FIFO bytes stored*

is reduced by one byte. Similarly, for every byte that it WRITTEN from the FIFO, the count of the number of FIFO bytes stored is increased by one byte.) The motivation for combining a video first-in-first out (FIFO) memory with a first input counter and a first output counter is, for each clock cycle, to monitor for preventing overflow threshold condition, data overflow and underflow problems in the FIFO, a time-buffer to compensate for different systems components that operate on different data or clock rates (Column 1, lines 9-57; Abstract). Duzan is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing MPEG high-definition video machines, to combine the benefits of a video first-in-first out (FIFO) memory, as Wang discloses, with first input and first output counters, as Duzan teaches, to monitor the FIFO overflow and underflow during each FIFO clock cycle.

6. Regarding claim 3, Wang discloses a raster engine of claim 2, wherein the control logic system provides the underflow signal (See above).

Wang does not disclose to a host processor in the computer system. Valmiki teaches a video controller raster engine in the computer system (Figures 1-5, 46, Column 80, lines 37-68; Column 88, lines 34-65; Column 90, lines 31-43; Column 95, lines 30-67) that receives video data and renders formatted data (*...decoded MPEG signals or other format of digital video,* Column 5, lines 21-29) to a display in a computer system (Figure 1, element 22; Figure 2, element 58;) from the frame buffer via the host bus and to provide video data to a video pipeline (see above, Figure 4, element 82, Column 8, lines 5-6). The motivation for combining a video first-in-first out (FIFO) memory with a computer rendering system is to manage the priority of memory requests tasks in a high-definition video application (Column 53 through Column 70) in

order not to starve or overfill the display memory (Column 56, lines 2-9). Valmiki is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing MPEG high-definition video machines, to combine the benefits of a video first-in-first out (FIFO) memory, as Wang discloses, with a computer MPEG video rendering system, as Valmiki teaches, to manage priorities of memory requests in order not to starve or overfill the display memory.

7. Regarding claim 5, representative of claims 6, 8, 9, 18-24, and 26-28, Wang,Valmiki, Duzan disclose a raster engine of claim 4, wherein the raster engine comprises an underflow threshold value register programmable, and wherein the control logic system obtains the threshold value from the threshold value register (See above, Column 5, lines 5-6, 21-61, *drain rate, tDRAIN, drain rate register*; *threshold*, Figure 6, element 132, Column 8, lines 31-61), and compares the threshold value with the difference between the counter values (Figure 3, elements 88, 90, *THRSH, tDRAIN, compare to tDRAIN,* Figures 6, 7, Column 6-9; *when the difference,* Column 2, lines 5-10).

Wang discloses a counter that has a value indicative of video data obtained from the frame buffer (Figure 2, elements 16, 18, 32, 56, 58, 78, *read and write pointers*, Column 4, lines 25-34); a counter (Figure 3, element 84) that has a value indicative of video data, provided to the video [memory] (Figure 3, elements 16, [**note element 62**], *pixel data,* 68, 80, ***indicates*** *the entry status,* Column 5, lines 22 through Column 6, line 66); and a control logic system (Figure 2, elements 78,) associated with the FIFO memory, that provides an underflow (and overflow)

indication (Figure 2, see Frame buffer above, *fill and drain standpoint,* Column 5, lines 22-26; *underflow (and overflow)*, Column 6, lines 65-66).

Wang discloses performing a comparison [based on] input and output counter values and that the underflow indication is controlled according to counter values (see above, *threshold watermark,* Column 8, lines 21-30).

Wang does not disclose to a host processor in the computer system. Valmiki teaches a video controller raster engine in the computer system (Figures 1-5, 46, Column 80, lines 37-68; Column 88, lines 34-65; Column 90, lines 31-43; Column 95, lines 30-67) that receives video data and renders formatted data (*...decoded MPEG signals or other format of digital video,* Column 5, lines 21-29) to a display in a computer system (Figure 1, element 22; Figure 2, element 58;) from the frame buffer via the host bus and to provide video data to a video pipeline (see above, Figure 4, element 82, Column 8, lines 5-6). The motivation for combining a video first-in-first out (FIFO) memory with a computer rendering system is to manage the priority of memory requests tasks in a high-definition video application (Column 53 through Column 70) in order not to starve or overfill the display memory (Column 56, lines 2-9). Valmiki is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing MPEG high-definition video machines, to combine the benefits of a video first-in-first out (FIFO) memory, as Wang discloses, with a computer MPEG video rendering system, as Valmiki teaches, to manage priorities of memory requests in order not to starve or overfill the display memory.

Wang does not disclose a first input counter nor a first output counter. Duzan teaches a first input [READ to the FIFO] counter and a first output [WRITE from the FIFO] counters

(Figure 2, elements 80 and 90, Column 3, lines 48-62, *Each clock cycle defines a FIFO memory period. For every byte that is READ from the FIFO, a count of the number of FIFO bytes stored is reduced by one byte. Similarly, for every byte that it WRITTEN from the FIFO, the count of the number of FIFO bytes stored is increased by one byte.*) The motivation for combining a video first-in-first out (FIFO) memory with a first input counter and a first output counter is, for each clock cycle, to monitor for preventing overflow threshold condition, data overflow and underflow problems in the FIFO, a time-buffer to compensate for different systems components that operate on different data or clock rates (Column 1, lines 9-57; Abstract). Duzan is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing MPEG high-definition video machines, to combine the benefits of a video first-in-first out (FIFO) memory, as Wang discloses, with first input and first output counters, as Duzan teaches, to monitor the FIFO overflow and underflow during each FIFO clock cycle.

8. Regarding claim 7, representative of claims 10, 11, 29, Wang discloses a raster engine of claim 6, wherein the FIFO memory obtains video data from the frame buffer according to a [memory] clock and provides video data to the pipeline (Column 2, line 34-35) according to a video clock, Column 1, lines 52-62) and wherein the underflow signal indicates an existing underflow condition when the counter values (See claims 2, 6, above).

Wang does not disclose to a host processor in the computer system. Valmiki teaches a video controller raster engine in the computer system (Figures 1-5, 46, Column 80, lines 37-68; Column 88, lines 34-65; Column 90, lines 31-43; Column 95, lines 30-67) that receives video data and renders formatted data (*...decoded MPEG signals or other format of digital video,*

Column 5, lines 21-29) to a display in a computer system (Figure 1, element 22; Figure 2, element 58;) from the frame buffer via the host bus and to provide video data to a video pipeline (see above, Figure 4, element 82, Column 8, lines 5-6). The motivation for combining a video first-in-first out (FIFO) memory with a computer rendering system is to manage the priority of memory requests tasks in a high-definition video application (Column 53 through Column 70) in order not to starve or overfill the display memory (Column 56, lines 2-9). Valmiki is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing MPEG high-definition video machines, to combine the benefits of a video first-in-first out (FIFO) memory, as Wang discloses, with a computer MPEG video rendering system, as Valmiki teaches, to manage priorities of memory requests in order not to starve or overfill the display memory.

Wang discloses counter values, thresholds, and three clock cycles (See above, Column 2, lines 35-36) but does not disclose first in/output counters and for at least two cycles of the [memory] clock. Duzan teaches first in/output counters and for each clock cycle (Column 1, lines 9-57) and a first input [READ to the FIFO] counter and a first output [WRITE from the FIFO] counters (Figure 2, elements 80 and 90, Column 3, lines 48-62, *Each clock cycle defines a FIFO memory period. For every byte that is READ from the FIFO, a count of the number of FIFO bytes stored is reduced by one byte. Similarly, for every byte that it WRITTEN from the FIFO, the count of the number of FIFO bytes stored is increased by one byte.*) The motivation for combining a video first-in-first out (FIFO) memory with a first input counter and a first output counter is, for each clock cycle, to monitor for preventing overflow threshold condition, data overflow and underflow problems in the FIFO, a time-buffer to compensate for different

systems components that operate on different data or clock rates (Column 1, lines 9-57; Abstract). Duzan is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing MPEG high-definition video machines, to combine the benefits of a video first-in-first out (FIFO) memory, as Wang discloses, with first input and first output counters, as Duzan teaches, to monitor the FIFO overflow and underflow during each FIFO clock cycle.

Claim Rejections - 35 USC § 103

9. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al, U.S. Patent 5,953,020, Valmiki et al, U.S. Patent 6,661,422, Duzan, U.S. Patent 5,214,607 as applied to claim 1 above, and further in view of Rudin, et al, U.S. Patent 5,959,640 and Reddy, U.S. Patent 6,195,079.

10. Regarding claim 12, representative of claims 15-16, Wang, Valmiki and Duzan disclose a raster engine of claim 1, further comprising: an input counter value indicative of video data obtained from the frame buffer; and an output counter having output counter value indicative of video data provided to the video pipeline; wherein the raster engine selectively performs operation with the FIFO memory to provide video data to the video pipeline represented by the counter values; and wherein the control logic system provides an underflow indication according to the input and output counter values (see above).

Wang does not disclose having a second input, second output, providing first and second video data to the video pipeline, nor do they disclose dual scan operation with the memory providing interleaved video. Rudin discloses dual scan operation and interleaved video memory

(Column 5, lines 14 – 30). The motivation for combining a video first-in-first out (FIFO) memory with dual scan and interleaved memory operations, as Rudin further teaches, is for display flexibility, particularly in LCD displays, and lower power consumption (Rudin, Column 1, lines 20-27, 48-50). Rudin is evidence that at the time of the invention, it would have been obvious for one skilled in the art of display controllers to combine the advantages of a video first-in-first out (FIFO) memory, as Wang discloses, with LCD displays needing low power consumption available with dual display and interleaved memory operation, as Rudin teaches.

Reddy discloses a first and second input and outputs (*cathode ray tube, computer system memory or from an input device;* Column 1, lines 26-39; Column 2, lines 33-36; Figure 3, Column 6, lines 9-20, 59-66; Column 8, lines 48-50; Column 11, lines 56-60). The motivation for combining a video first-in-first out (FIFO) memory with multiple inputs and outputs is to handle multiple display types (both LCD and CRT) and display requirements (Column 1, lines 52-66). Reddy is evidence that at the time of the invention it would have been obvious to one skilled in the art of display design to incorporate the advantages of video control features, as Wang disclose, that operate on multiple types of displays, as Reddy teaches, requiring first and second inputs and outputs due to the different display-type principles of operation.

11. Regarding claim 13, representative of claim 14, Wang, Valmiki, Duzan disclose a raster engine of claim 12, wherein the underflow indication comprises an underflow signal indicating at least one of an existing underflow condition, an anticipated underflow condition, and a raster engine lockup condition (see Claim 2 above).

Prior Art Not Used

Cutler, U.S. Patent 3,603,725, video Frame buffer FIFO control using counters, threshold circuit.

Kullander, U.S. Patent 5,315,587, watermark control of a buffer using in/output counters

Response to Arguments

12. The Applicant argues that references do not teach or disclose the features of claim 1.

The Office has reviewed the matter, and the Examiner agrees. Better art is now provided that does disclose the features of claim 1, namely, the FIFO underflow indication with first input and output counter values (See Wang, Column 5, lines 22 through Column 6, line 66; Duzan, Figure 2, elements 80 and 90, Column 3, lines 48-62).

13. The Applicant asserts that "Neither Rudin et al. nor Reddy overcome the deficiencies of Kuchkuda et al. and Nishiyama with respect to independent claim 1." (Page 12, last paragraph).

The Examiner respectfully replies that, in the claims 12-16 however, Rudin and Reddy teach the features of a second input, second output, providing first and second video data to the video pipeline, dual scan operation with the memory providing interleaved video for the purpose of low power consumption and multiple display types.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or FAX'd to:

(703) 872-9314 (for Technology Center 2600 only)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

***March 6, 2004

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600